REMARKS

Applicants respectfully requests consideration and allowance of claims 1, 3-9, 11-16, 18-21, 23-26, and 28-35 that are pending in the above-identified patent application. Applicants have amended claims 1, 3-5, 9, 11-13, 16, 18-21, 23-26, 28-35 and canceled claim 22 in this response. No new matter has been added by way of these amendments.

I. Claim Objections

At page 2 of the Office Action, the Examiner has objected to claims 1, 5, 9, 13, 16 20, 21, 25, 26, and 30 for informalities. Specifically, the Examiner alleges that "by combinations each" is unclear as recited in the claims. Applicant has amended the claims to recite "defined by combinations, wherein each comprises" as based on the Examiner's suggestion.

Further, the Examiner has objected to claim 22 as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant has cancelled claim 22 in response to this objection.

In view of the above, Applicant submits that the Examiner's claim objections have been overcome, and respectfully requests that the Examiner's claim objections be withdrawn.

II. Rejection of Claims 26, 28-30, 35 Under 35 U.S.C. §101:

At numbered part 5 of the Office Action, the Examiner has rejected claims 26, 28-30, and 35 under 35 U.S.C. §101 as allegedly being directed towards non-statutory subject matter. Applicant respectfully traverses this rejection and requests that the rejection be withdrawn in view of the amended independent claims 26 and 30.

In the detailed action, the Examiner states that, in reference to the recitation in claims 26 and 30 of a "processor readable storage medium," there is no antecedent basis in the specification for this part in the claim language. In short, the Examiner believes that the specification of the present application does not disclose a processor readable storage medium. However, support for a "processor readable storage medium" can be found in the specification and figures of the present application. Specifically, the memory unit 300 that is shown in Figure 1 is a processor readable

storage medium, as processor memory is considered to be a processor readable storage medium in that it is a medium for storage and the processor is capable of reading it. (*See,* also Applicant's specification as filed page 6 line 24 and page 7 lines 20-21). As a memory unit is clearly shown in the figures of the present application, Applicant contends that the claim language "processor readable storage medium" has antecedent basis and therefore, this rejection should be withdrawn.

III. Rejection of Claims 1, 5-8, 9, 13-16, 20-22, 25-26, and 30 Under 35 U.S.C. §103(a):

At numbered parts 8-20 of the subject Office Action, the Examiner has rejected claims 1, 5-8, 9, 13-16, 20-22, 25-26, and 30 under 35 U.S.C. §103(a) as being unpatentable over Rusu et al. (U.S. 7,111,178). Applicant respectfully requests that this rejection be withdrawn as Rusu et al. fails to teach or suggest all aspects recited in the subject amended claims.

The claimed subject matter generally relates to a processor comprising a plurality of subprocessors. In particular, independent claim 9 recites: a table that lists a plurality of operation points defined by combinations, wherein each comprises: a) the number of subprocessors in operation; and b) one of a plurality of operating frequencies available for use by switching; and a control unit, which consults the table and switches between the operation points in accordance with the measured temperature. Independent claims 13, 16, 20, 21, 25, 26 and 30 recite similar features.

Similarly independent claim 1 recites: consulting a table that lists a plurality of operation points defined by combinations, wherein each comprises: a) the number of a plurality of subprocessors formed inside a processor that are in operation; and b) one of a plurality of operating frequencies available for use by switching.

Rusu et al. does not teach or suggest such aspects.

The Examiner alleges in his rejection of claim 1 that Rusu et al. teaches a method of controlling a processor comprising "consulting a table that lists a plurality of operations points defined by combinations each comprising one of a plurality of operating frequencies available for use by switching so as to switch between the operation points in accordance with a temperature." The Examiner has equated a fuse array 214 in Rusu et al., which is memory located on the processor, with the table of recited in the subject independent claims. However, Applicant respectfully

disagrees with the Examiner that Rusu et al. disclsoes a table that comprises the number of the plurality of subprocessors in operation and one of a plurality of operating frequencies available for use by switching. According to Rusu et al., the fuse array 214 "contains information as to operating points based on different frequency and voltage points" (*See*, Rusu et al., Col. 6, lines 34-36). As it is directed to voltage points, Rusu et al. is silent as to the fuse array 214 containing a combination of different frequencies and the subprocessors in operation.

Applicant respectfully acknowledges the Examiner's concession that Rusu et al. "does not explicitly teach each combination comprising the number of processing blocks formed inside a processor and in operation." The Examiner alleges, on the other hand, that this point is obvious because a processor needs processing blocks to function and points to the core and other functional units of the processor in Rusu et al. In response, Applicant submits that Rusu et al. does not disclose a multiprocessor comprising a plurality of subprocessors as currently recited in all the independent claims.

In accordance with the claimed subject matter, the operation points contained within a table are comprised of the combination of an operating frequency of the processor and the number of subprocessors in the processor that are in operation. As the table is given with reference to a plurality of the subprocessors, it is required that more than just one processor unit exist, since the claimed subject matter seeks to enhance performance of a multiprocessor system by switching the availability of processors in accordance with their respective temperatures. According to the structure in Rusu et al., as indicated in Figures 1 and 2, each processor and subprocessor would need to have their own array with operating frequencies (as shown from Figure 1, where multiple processors 102 are connected on a processor bus 110, and, from Figure 2, where each processor 102 has a fuse array 214). Therefore, it can be concluded that Rusu et al. fails to disclose a single table for the entire processor with a plurality of subprocessors, as recited in amended independent claims. In view of the above, Rusu et al. fails to teach or suggest a table that comprises the number of the plurality of subprocessors in operation and one of a plurality of operating frequencies available for use by switching.

In view of at least the foregoing, it can be concluded that the cited art does not teach or suggest all aspects recited in the subject independent claims. Hence, Applicant respectfully requests

that the Examiner's § 103 claim rejections be withdrawn with respect to these independent claims and claims 5, 9, 13, 16, 20, 21, 25, 26 and 30 depending therefrom.

IV. Rejection of Claims 3, 11, 18, 23 and 28 Under 35 U.S.C. §103(a):

At numbered parts 21-22 of the Office Action, the Examiner has rejected claims 3, 11, 18, 23 and 28 under 35 U.S.C. §103(a) as allegedly being unpatentable over Rusu et al. and Guo et al. (U.S. 20050071843). Applicants traverse the rejection and submit that this rejection should be withdrawn for at least the following reasons. Rusu et al. in view of Guo et al., alone or in combination, fail to teach or suggest all aspects recited in the independent claims from which the subject claim depend.

In particular, claims 3, 11, 18, 23 and 28 depend from independent claims 1, 9, 16, 21 and 26 respectively. The deficiencies of the Rusu et al. as concerns these independent claims were discussed above. As the teachings of the Guo et al. that the Examiner alleges is combinable with Rusu et al. do not cure such deficiencies, Applicants respectfully request that the obviousness rejection of the subject claims be withdrawn. More particularly, Guo et al. relates to scheduling jobs in a multiprocessor machine. The jobs are scheduled by comparing resource requirements of jobs against resources available to particular CPUs. However, alone or in combination with Rusu et al. it fails to teach or suggest consulting a table that lists a plurality of operation points defined by combinations wherein each combination comprises: a) the number of processing blocks formed inside a processor and in operation; and b) one of a plurality of operating frequencies available for use by switching, so as to switch between the operation points in accordance with a temperature or a control unit which consults the table and switches between the operation points in accordance with the measured temperature. In view of at least the foregoing, it is requested that this rejection should be withdrawn.

V. Rejection of Claims 4, 12, 24, 29 and 31-35 Under 35 U.S.C. §103(a):

At numbered parts 23-25 of the Office Action, the Examiner has rejected claims 4, 12, 24, 29 and 31-35 under 35 U.S.C. §103(a) as being obvious over a combination of Rusu et al. and Luick (U.S. 20030229662). This rejection should be withdrawn for at least the following reasons. Rusu et

al. and Luick alone or in combination do not teach or suggest all aspects recited in independent claims 1, 9, 21, 26, and 30 from which the subject claims depend respectively.

The deficiencies of the Rusu et al. as concerns these independent claims were discussed above. As the teachings of the Luick that the Examiner alleges is combinable with Rusu et al. do not cure such deficiencies, Applicants respectfully request that the obviousness rejection of the subject claims be withdrawn. More particularly, Luick relates to eliminating hot spots on processor chips in a symmetric multiprocessor (SMP) computer system. When a hot spot occurs on a processor, tasks are swapped to another processor prior to the localized temperature becoming too hot. Moving of tasks to processors that have data affinity with the processor reporting a hot spot is one of the considerations. Further considerations include prioritizing unused processors and those processors that have not recently reported a hot spot. (*See,* Luick Abstract). However, alone or in combination with Rusu et al. it fails to teach or suggest consulting a table that lists a plurality of operation points defined by combinations wherein each combination comprises: a) the number of processing blocks formed inside a processor and in operation; and b) one of a plurality of operating frequencies available for use by switching, so as to switch between the operation points in accordance with a temperature or a control unit which consults the table and switches between the operation points in accordance with the measured temperature. In view of at least the foregoing, it is requested that this rejection should be withdrawn.

Conclusion:

In view of the foregoing, Applicant respectfully submits that the instant application is in condition for allowance. Early and favorable action is earnestly solicited.

In the event there are any fees due and owing in connection with this matter, please charge same to our Deposit Account No. 11-0223.

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